IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yew	Docket No:	TI-26239.1
Serial No:	10/612,129	Examiner:	Cao, Phat X.
Filed:	7/2/2003	Art Unit:	2814

For: DIRECT ATTACHMENT OF SEMICONDUCTOR CHIP TO ORGANIC SUBSTRATE

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on 2-3-05

Tommie Chambers

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final rejection mailed August 6, 2004, and the Advisory Action mailed October 29, 2004.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-32 were originally filed and Claims 16-32 were cancelled. Thus, the subject matter of the instant appeal is Claims 1-15.

STATUS OF AMENDMENTS

Claims 1-15 remain in the application for consideration of the Board.

A response after final was mailed on October 21, 2004, amending no claims.

Applicants assume that it has been entered since the Examiner indicated in the Advisory Action that the response had been considered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention provides a method of assembling a semiconductor device; it especially relates to high density, high speed integrated circuits in packages which have an outline similar to the integrated circuit chip itself, and a low profile. These circuits can be found in many device families such as processors, digital and analog devices, memory and logic devices, high frequency and high power devices, especially in large chip area categories. The invention helps to alleviate the space constraints in continually shrinking applications such as cellular communications, pagers, hard disk drives, laptop computers and medical instrumentation.

In accordance with the present invention, an preactivation method is provided for the protective polymer layer on the surface of integrated circuit chips which imparts adhesiveness to the polymer layer. Furthermore, an electrically insulating substrate is provided, comprising a plurality of conductive routing strips integral with the substrate.

This substrate is directly attached to the preactivated polymer layer. The preactivation comprises a plasma exposure of the polymer layer for increasing the surface roughness and creating molecular radicals consisting of chemically unsaturated bonds.

The present invention to be applicable to a variety of different semiconductor chip-scale package (CSP) designs, for example: Chip attached directly to board, chip assembled to board with interim metal layer, center-line bonding, peripheral bonding, wire bonding, and flip-chip solder bonding.

The present invention is to provide a low-cost method and system for assembling chip-scale devices in thin overall profile.

The present invention is to improve product quality by adhesion uniformity, and to enhance reliability assurance by controlling mechanical stress, minimizing moisture absorption, and general in-process control at no extra cost.

The invention is to introduce assembly concepts for thin profiles which are flexible so that they can be applied to many families of semiconductor products, and are general so that they can be applied to several future generations of products.

The method includes attaching the chip to the organic substrate includes positioning the substrate in contact with the preactivated polymer layer on the chip. The chip can be mounted on a stage where heat is applied to the chip and the substrate. Also, force may be applied between the chip and the substrate. In one embodiment of the invention, the temperature applied to the chip is between 150 and 350 °C and may preferably be about 200 ° C. In another embodiment of the invention, the force applied between the chip and the substrate may be between 5 and 7 kg and preferably about 5.5 kg. The force may be applied for between 2 and 10 s and preferably for about 5 s.

A metal layer is disposed on the surface of the substrate facing the chip prior to attaching this surface to the preactivated polymer layer on the chip. When heat is

applied to the chip and the substrate, the temperature applied may be between 150 and 350 °C and may preferably be about 200 °C. When force is applied between the chip and the substrate, the force may be between about 1.5 and 7.0 kg and preferably be about 3 kg. The force may be applied for between 2 and 10 s and preferably for about 5 s.

A transfer molding process replaces conventional encapsulation methods, with the process parameters (temperature, time, pressure, transfer, curing, etc.) modified in order to optimize them relative to the system and materials parameters.

GROUNDS OF REJECTION

The two grounds on appeal are first whether Claims 1, 2, 4, and 7-15 are unpatentable under 35 U.S.C. § 103 over Lee in view of Lupinski; and second whether Claims 5 and 6 are unpatentable under 35 U.S.C. § 103 over Lee, Lupinski, and Hiroshi.

ARGUMENTS

It is respectfully submitted that Lee does not disclose or suggest the presently claimed invention including the plurality of contact pads disposed on the first surface of the substrate and a second surface of the substrate being directly attached to the preactivated polymer level.

Applicants agree with the Examiner that Lee does not disclose the protecting adhesive layer being a protective polymer having been preactivated.

It is respectfully submitted that Lupinski does not disclose or suggest the presently claimed invention including a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the preactivated polymer level.

Lupinski does not disclose a preactive layer being used with a insulating substrate that bears a relationship to contact pads.

Furthermore, whether or not Hiroshi discloses forming a metal layer on a protective adhesive layer and whether one of ordinary skill in the art would have modified either Lee or Lupinski is of no moment since the resulting construction would in no way disclose or suggest the presently claimed invention.

The Examiner alleges that Applicants argument has no immediate apparent relevance to the issues presented by the rejection since the Applicant cannot show obviousness by attacking reference individually where the rejection is based on the combination of references.

Notwithstanding the allegations of the Examiner, none of the references discloses a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the preactivated polymer level.

Applicants respectfully submit that the Examiner has used impermissible hindsight in order to reject the Applicant's claims. More particularly, the Examiner has pieced together the teachings of the prior art using the instant specification as a guide.

Such rejections are clearly impermissible.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-15 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

APPENDIX

Claim 1 (original): A semiconductor device comprising:

an integrated circuit chip having an active and a passive surface, said active surface

including a protective polymer layer having been preactivated to impart adhesiveness, and at least one bonding pad;

an electrically insulating substrate having first and second surfaces;

a plurality of electrically conductive routing strips integral with said substrate;

a plurality of contact pads disposed on said first surface of said substrate, at least one of said contact pads electrically connected with at least one of said routing strips;

said second surface of said substrate being directly attached to said preactivated polymer layer; and

bonding wires electrically connecting said at least one bonding pad to at least one of said contact pads.

Claim 2 (original): The semiconductor device according to Claim 1 wherein said polymer layer is a polyimide layer.

Claim 3 (previously presented): A semiconductor device comprising:

an integrated circuit chip having an active and a passive surface, said active surface

including a protective polymer layer having been preactivated to impart adhesiveness, and at least one bonding pad;

an electrically insulating substrate having first and second surfaces;

a plurality of electrically conductive routing strips integral with said substrate;

a plurality of contact pads disposed on said first surface of said substrate, at least one of said contact pads electrically connected with at least one of said routing strips;

said second surface of said substrate being directly attached to said preactivated polymer layer; and

bonding wires electrically connecting said at least one bonding pad to at least one of said contact pads,

wherein said preactivation comprises plasma exposure of said polymer layer for increasing the surface roughness and creating molecular radicals comprising chemically unsaturated bonds.

Claim 4 (original): The semiconductor device according to Claim 1 wherein said substrate is made of organic material and is selected from a group consisting of FR-4, FR-5 and BT resin.

Claim 5 (original): The semiconductor device according to Claim 1 wherein a metal layer is disposed on said second surface of said substrate prior to attaching said second surface to said preactivated polymer layer on said chip.

Claim 6 (original): The semiconductor device according to Claim 5 wherein said metal layer is selected from a group consisting of copper, copper alloy, iron-nickel alloy, invar and gold.

Claim 7 (original): The semiconductor device according to Claim 1 wherein said at least one bonding pad is disposed at the periphery of said chip.

Claim 8 (original): The semiconductor device according to Claim 7 wherein said contact pads are disposed around the periphery of said substrate.

Claim 9 (original): The semiconductor device according to Claim 1 wherein said at least one bonding pad is disposed at the centerline of said chip.

Claim 10 (original): The semiconductor device according to Claim 9 wherein said substrate has an opening and said contact pads are disposed along said opening.

Claim 11 (original): The semiconductor device according to Claim 1 wherein encapsulating material covers said bonding wires, said at least one bonding pad and said contact pads.

Claim 12 (original): The semiconductor device according to Claim 1 wherein said first surface of said substrate further comprises a plurality of assembly pads, at least one of said assembly pads electrically connected with at least one of said routing strips.

Claim 13 (original): The semiconductor device according to Claim 12 further including at least one solder ball located on at least one of said assembly pads disposed on said first surface.

Claim 14 (original): The semiconductor device according to Claim 1 wherein said chip and said substrate have substantially the same outlines.

Claim 15 (original): The semiconductor device according to Claim 1 wherein said integrated circuit chip comprises silicon, silicon germanium, gallium arsenide or any other semiconductor material used in electronic device production.

Claims 16-32 (cancelled)

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.